Hamza Omar

Resumé – Curriculum Vitaé

371 Fairfield Way, Lab 427
Storrs, CT, 06269
✉ *hamza.omar@uconn.edu*
www.hamza-omar.grad.uconn.edu

Interests

Computer Architecture, Architectural Security & Resiliency, System-level Security, Hardware Accelerators, Approximate Computing, Graph and Machine Learning Algorithms, and Parallel Programming.

Education

2017–2020 **PhD. Electrical and Computer Engineering**, *University of Connecticut*, Storrs, CT, USA.
Graduate Research Assistant in the Computer Architecture Group.
Thesis: *"Dynamic Hardware Isolation for Efficient Resiliency & Security in Multicore Architectures"*.

2015–2017 **MSc. Electrical Engineering**, *University of Connecticut*, Storrs, CT, USA.
Graduate Research Assistant in the Computer Architecture Group.
Thesis: *"Towards Efficient Computation in Real-Time Systems"*.

2011–2015 **BSc. Electrical Engineering**, *University of Engineering & Technology (UET)*, Lahore, Pakistan.
Thesis: *"WiFi based Home Automation using Master-Slave Communication"*.

Courses Advanced Computer Architecture, Multicore Architecture, Parallel Programming, Algorithms Design, Networked Embedded Systems, Secure Computation and Storage, Hardware Security, Machine Learning, Digital Image Processing, Formal Verification Methods, Mobile Robotics, Advanced Digital System Design.

Research Experience

2015–Present **Graduate Research Assistant, University of Connecticut (UConn)**.
Research Adviser: Prof. Omer Khan.

1. Leveraging Hardware Isolation for Efficient Security & Resiliency in Multicore Processors.
Collaborators: National Science Foundation (NSF), Semiconductor Research Corporation (SRC).
- Devised a novel multicore architecture that employs a *spatio-temporal* execution model for efficient mitigation of microarchitecture state attacks and effective resiliency against soft-error perturbations.
- Prototyped the architecture (framework) on a real *Tilera® Tile-Gx72™* multicore processor.
- Validation on a Xilinx VCU118 FPGA using the OpenPiton cache coherent multicore. The development of the RTL design is in progress.
- **Employed Tools**: *Tilera®* TMC APIs, C/C++, Python, Xilinx Vivado, and Linux.
- **Skills Acquired**: Performance Analysis, Interactive Application Development, and FPGA Modeling.

2. A Cross-Layer Resilient Architecture to Tradeoff Program Accuracy and Resilience Overheads.
Collaborators: National Science Foundation (NSF).
- Developed a multicore architecture for resiliency that selectively employs core-level redundant execution.
- Devised a fault injection tool to analyze the application output accuracy.
- **Employed Tools**: Graphite Multicore Simulator, Intel's Pin Instrumentation Tool, C/C++, Python, and Linux.
- **Skills Acquired**: Performance Analysis, Multicore Simulator Modeling and Fault Injection Model Development.

3. Reducing Oblivious RAM overheads by Efficient Memory Bandwidth Utilization.
Collaborators: National Science Foundation (NSF), Connecticut Cyber-Security Center (C^3).
- Implemented and simulated a performance efficient ORAM scheme that ensures near-optimal load and capacity balancing across multiple on-chip memory controllers (and channels) to fully exploit available memory bandwidth.
- **Employed Tools**: Graphite Multicore Simulator, Intel's Pin Instrumentation Tool, C/C++, Python, and Linux.
- **Skills Acquired**: Performance and Multicore Simulator Modeling.

Professional Work Experience

Summer 2018 **Research Intern, NXP Semiconductors**, *Austin, Texas, USA*.
- Developed and analyzed the 2D-UESPRIT imaging radar algorithm for self-driving autonomous systems.
- **Employed Tools**: NXP® RISC-V Multicore Simulator, Eigen Library, Matlab, C/C++, NewLib, and Linux.
- **Skills Acquired**: Radar Application Development, Multicore Simulator Modeling, Performance Bottleneck Analysis, Cache and Memory Access Optimization.

Summer 2014 **Research Intern, Al-Khawarizmi Research Institute of Computer Sciences (UET)**, *Pakistan*.
- Extracted the $H.264$ encoded video from a .MP4 video stream and tracked an event of interest using probabilistic and machine learning approaches.
- **Employed Tools**: Visual Studio, C/C++, and Matlab.
- **Skills Acquired**: Machine Learning Principles, Performance Analysis, and .MP4 Video Analysis.

Key Publications (Full Publication List)

S&P 2020 **H. Omar**, V. Garg, M. van Dijk, O. Khan, *"Unifying Hardware Root-of-Trust in Secure Processor Architectures"*, *IEEE Symposium on Security and Privacy*, 2020. (*Under Submission*)

TC 2020 **H. Omar**, O. Khan, *"OPTIMUS: A Security-Centric Dynamic Hardware Partitioning Scheme for Processors that Prevent Microarchitecture State Attacks"*, *IEEE Transactions on Computers*, 2020. (*Under Review*)

HPCA 2020 **H. Omar**, O. Khan, *"IRONHIDE: A Secure Multicore that Efficiently Mitigates Microarchitecture State Attacks for Interactive Applications"*, *IEEE Symposium on High-Performance Computer Architecture*, 2020.

CAL 2018 **H. Omar**, H. Dogan, B. Kahne, O. Khan, *"Multicore Resource Isolation for Deterministic, Resilient and Secure Concurrent Execution of Safety-Critical Applications"*, *IEEE Computer Architecture Letters*, 2018.

ICCD 2018 **H. Omar**, S. Kamran, L. Ren, M. van Dijk, O. Khan, *"Breaking the Oblivious RAM Bandwidth Wall"*, *IEEE International Conference on Computer Design*, 2018.

TECS 2018 **H. Omar**, Q. Shi, M. Ahmad, H. Dogan, O. Khan, *"Declarative Resilience: A Framework for Multicore Architectures that trades off Program Accuracy for Efficient Execution"*, *ACM Transactions on Embedded Computing Systems*, 2017.

Technical Skills

Modeling Tools: Multicore Simulators (Graphite, Quarq)

Development Tools: Xilinx Vivado, Git, SVN, Atmel Studio, Visual Studio, Pthread Library, Windows, Linux, Microsoft Office, Eclipse, MATLAB, Labview, Proteus, LaTeX.

Programming & Scripting: C/C++, Python, Ruby on Rails, HTML/CSS, MakeFile.

Hardware Designing: Verilog, VHDL

Research Grants

CHEST 2019 Helped author grant with Omer Khan, *"Leveraging Hardware Isolation for Secure Execution of Safety-Critical Applications in Distributed Systems"*, Center for Hardware and Embedded Systems Security and Trust.

NSF 2019 CNS-1929261 Helped author grant with Omer Khan, *"A Secure Processor that Exploits Multicore Parallelism While Protecting Against Microarchitecture State Attacks"*, Secure and Trustworthy Cyberspace:CORE, Small.

Teaching Experience

Spring 2018 **Teaching Assistant**, *University of Connecticut* – Digital Systems Design (VHDL).

Fall 2017 **Teaching Assistant**, *University of Connecticut* – Microprocessor Application Laboratory.

Spring 2017 **Teaching Assistant**, *University of Connecticut* – Digital Systems Design (VHDL).

Awards and Honors

Summer 2019 **Research Fellowship Award** from the University of Connecticut.

2017 & 2018 **Best Teaching Assistant Award** from the University of Connecticut.

2014–2015 **Color of UET** from University of Engineering & Technology, Lahore, Pakistan.

2015 **Best Senior Year Technical Report Award** from the University of Engineering and Technology.

Summer 2013 **Best Intern Award** from Punjab Information Technology Board of Govt. of Punjab, Pakistan.

2009–2011 **National Talent Scholarship** from the Govt. of Pakistan.

2009 **Yousaf Wahab Award of Honor** from Lahore Diocesan Board of Education, Pakistan.

Reviewing Services

Conferences Indirect Reviewer for the following: ISCA, HPCA, ASPLOS, PACT, MICRO, IISWC, ICCD, and ISPASS.

Journals Direct External Reviewer for the following: TACO, TDSC, TC, and TECS.

Mentoring & Outreach Activities

Summer 2016, 2017 & 2019 — Mentored several students under the **Research Experience for Undergraduates (REU) program** at the University of Connecticut. The program targeted computer security education for undergraduates. The program targeted computer security education for undergraduates. Students included from diverse backgrounds, including students with disabilities.

2011–2013 **Visiting Motivational/Course Strategy Instructor**, Knowledge Inn Preparatory School, Pakistan.

Extracurricular Side Activities

2016–2019 **Vice-Captain** of the NFC soccer club in Connecticut.

Fall 2018 **Volunteer** at the New York University – World Science Festival.

2017–2019 UConn Racquetball **Singles** and **Doubles** Champion.

2013–2014 **Athlete of the year** at University of Engineering & Technology.

2013–2015 Former **Captain** of University of Engineering & Technology Soccer team.

2014–2015 **Co-Founder** of University of Engineering & Technology Photography Society, and IEEE Computer Society University of Engineering & Technology Chapter.

References

Omer Khan
Department of Electrical Engineering
University of Connecticut
Storrs, CT 06269
✉ khan@uconn.edu
☎ 860-486-2192

Marten van Dijk
Department of Electrical Engineering
University of Connecticut
Storrs, CT 06269
✉ vandijk@engr.uconn.edu
☎ 860-486-2689

Brian Kahne
Principal Engineer
NXP Semiconductors
Austin, TX, 78735.
✉ brian.kahne@nxp.com
☎ 512-933-8214

John Chandy
Department of Electrical Engineering
University of Connecticut
Storrs, CT 06269
✉ john.chandy@uconn.edu
☎ 860-486-5047